Sitronix

ST7921

96CH Segment Driver For Dot Matrix LCD

■ Features :

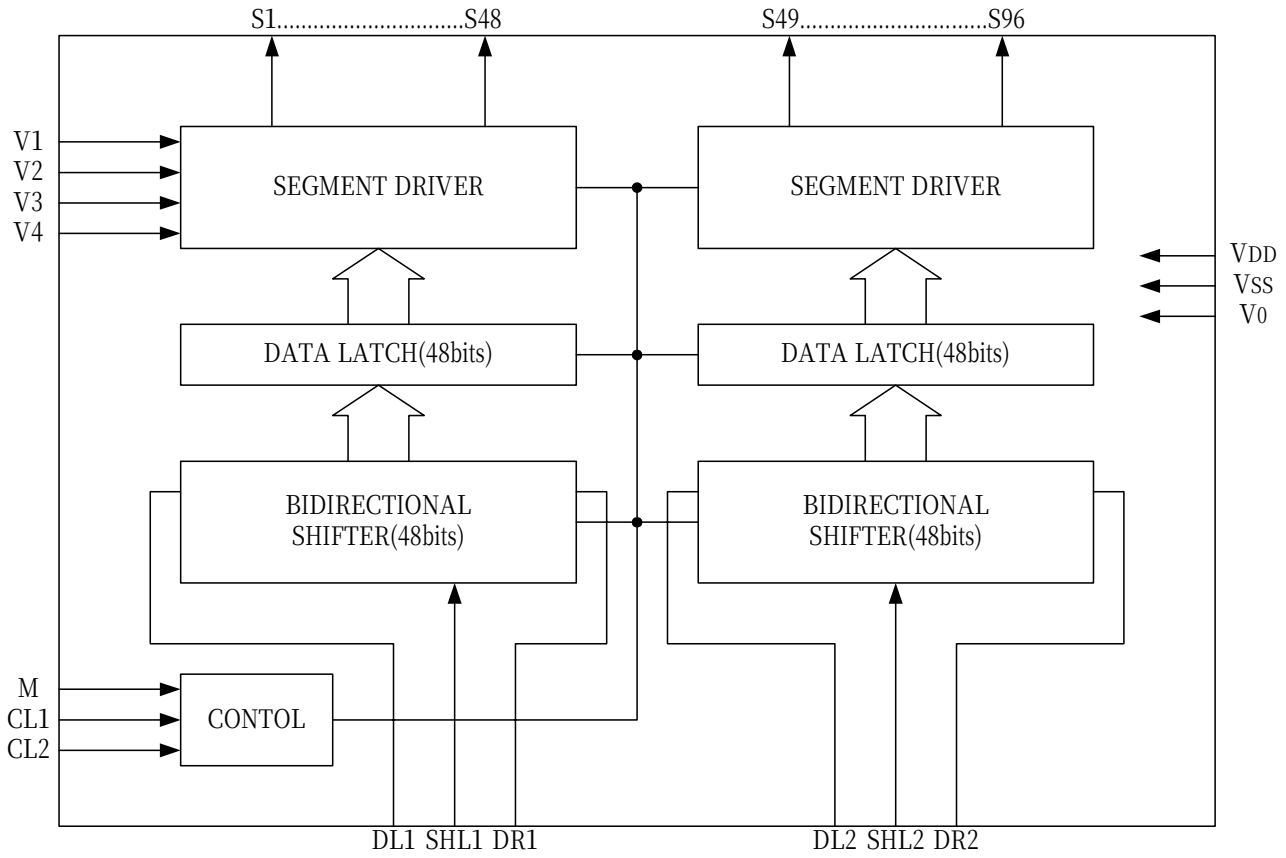
- Display driving bias : static to 1/5
- Power supply for logic : 2.7V ~ 5.5V
- Power supply for LCD voltage (V_0~V_{SS}) : 3V ~ 7V
- Dot matrix LCD driver with two 48 channel outputs
- Bias voltage (V0 ~ V4)
- Input/Output signals
  - Input : Serial display data and control pulse from controller IC
  - Output : 48 X 2 channels waveform for LCD driving

■ General Description :

ST7921 is a segment driver for dot matrix type LCD display. It features 96 channels with 48 X 2 bits bi-directional shift registers, data latches, LCD drivers and logic control circuits. It is fabricated by high voltage CMOS process with low current consumption.

The ST7921 can convert serial data received from an LCD controller, such as ST7920, into parallel data and send out LCD driving waveforms to the LCD panel. The ST7921 is designed for general purpose LCD drivers. It can drive both static and dynamic drive LCD. The LSI can be used as segment driver.

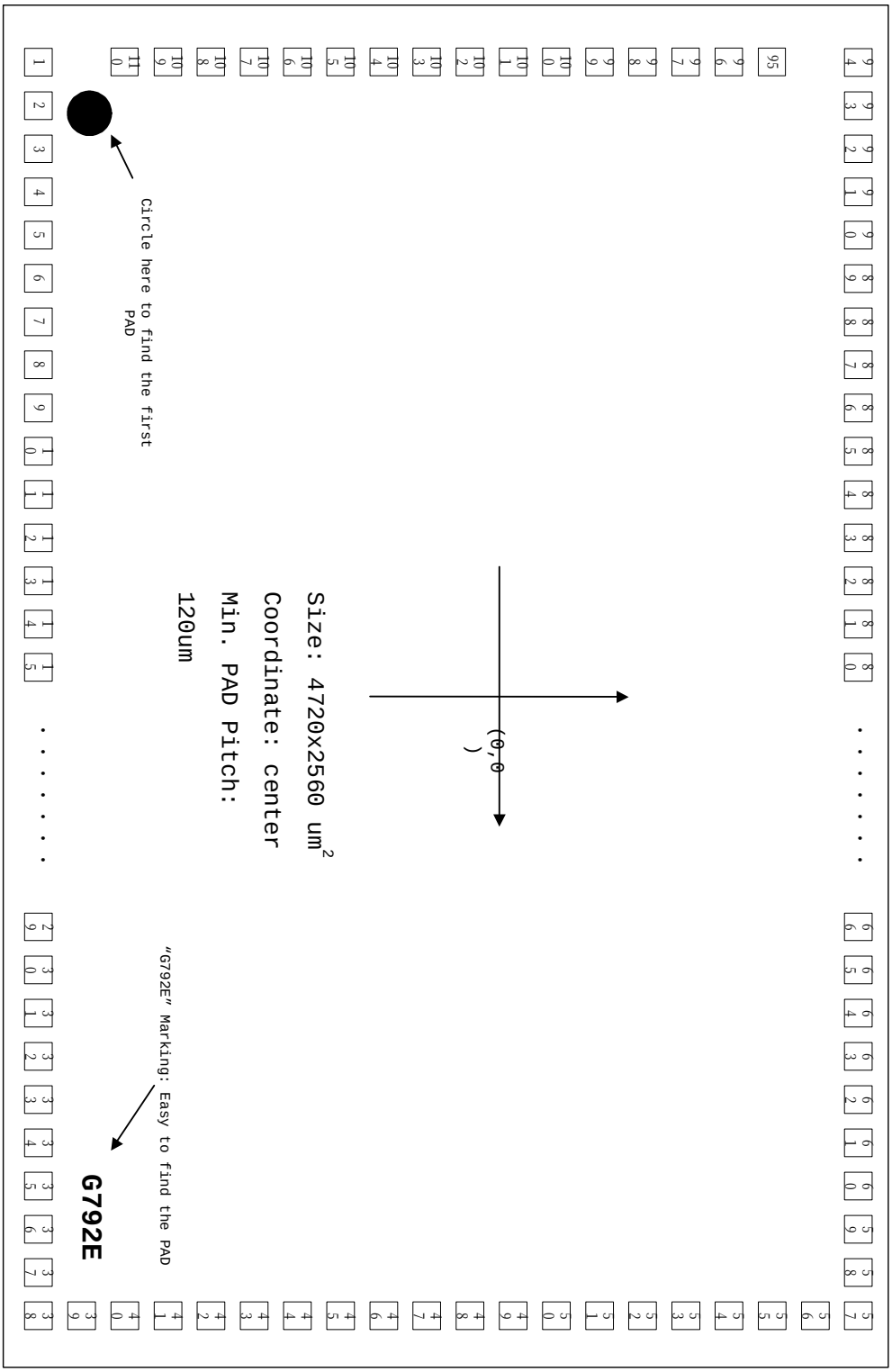
■ ST7921 Functional Block



■ Pin Description :

Pin Name	Purpose	Description	I/O
VDD	POWER	for logic	N/A
VSS	GROUND	for logic	N/A
V0 V2 V3	LCD Power	for LCD driving voltage	I
S1-S48	segment	LCD driver output for part 1	O
SHL1	direction	direction control for part 1 segments	I
DL1, DR1	data in /out	If SHL1 = 1 then DL1=out, DR1=in If SHL1 = 0 then DL1=in, DR1=out	I/O
S49-S96	segment	LCD driver output for part 2	O
SHL2	direction	direction control for part 2 segments	I
DL2, DR2	data in/out	If SHL2 = 1 then DL2=out, DR2=in If SHL2 = 0 then DL2=in, DR2=out	I/O
M	alternation	Alternate the LCD driving waveform	I
CL1	latch clock	latch the data after shift is completed	I
CL2	shift clock	shift the data into the segments	I

■ Pad Arrangement



*** chip substrate must connect to VSS**

■ Bonding Description

Pad No.	Pad Name	X	Y
1	S[50]	-2240	-1160
2	S[51]	-2110	-1160
3	S[52]	-1980	-1160
4	S[53]	-1860	-1160
5	S[54]	-1740	-1160
6	S[55]	-1620	-1160
7	S[56]	-1500	-1160
8	S[57]	-1380	-1160
9	S[58]	-1260	-1160
10	S[59]	-1140	-1160
11	S[60]	-1020	-1160
12	S[61]	-900	-1160
13	S[62]	-780	-1160
14	S[63]	-660	-1160
15	S[64]	-540	-1160
16	S[65]	-420	-1160
17	S[66]	-300	-1160
18	S[67]	-180	-1160
19	S[68]	-60	-1160
20	S[69]	60	-1160
21	S[70]	180	-1160
22	S[71]	300	-1160
23	S[72]	420	-1160
24	S[73]	540	-1160
25	S[74]	660	-1160
26	S[75]	780	-1160
27	S[76]	900	-1160
28	S[77]	1020	-1160

Pad No.	Pad Name	X	Y
29	S[78]	1140	-1160
30	S[79]	1260	-1160
31	S[80]	1380	-1160
32	S[81]	1500	-1160
33	S[82]	1620	-1160
34	S[83]	1740	-1160
35	S[84]	1860	-1160
36	S[85]	1980	-1160
37	S[86]	2110	-1160
38	S[87]	2240	-1160
39	S[88]	2240	-1030
40	S[89]	2240	-900
41	S[90]	2240	-780
42	S[91]	2240	-660
43	S[92]	2240	-540
44	S[93]	2240	-420
45	S[94]	2240	-300
46	S[95]	2240	-180
47	S[96]	2240	-60
48	S[48]	2240	60
49	S[47]	2240	180
50	S[46]	2240	300
51	S[45]	2240	420
52	S[44]	2240	540
53	S[43]	2240	660
54	S[42]	2240	780
55	S[41]	2240	900
56	S[40]	2240	1030

Pad No.	Pad Name	X	Y
57	S[39]	2240	1160
58	S[38]	2110	1160
59	S[37]	1980	1160
60	S[36]	1860	1160
61	S[35]	1740	1160
62	S[34]	1620	1160
63	S[33]	1500	1160
64	S[32]	1380	1160
65	S[31]	1260	1160
66	S[30]	1140	1160
67	S[29]	1020	1160
68	S[28]	900	1160
69	S[27]	780	1160
70	S[26]	660	1160
71	S[25]	540	1160
72	S[24]	420	1160
73	S[23]	300	1160
74	S[22]	180	1160
75	S[21]	60	1160
76	S[20]	-60	1160
77	S[19]	-180	1160
78	S[18]	-300	1160
79	S[17]	-420	1160
80	S[16]	-540	1160
81	S[15]	-660	1160
82	S[14]	-780	1160
83	S[13]	-900	1160
84	S[12]	-1020	1160

Pad No.	Pad Name	X	Y
85	S[11]	-1140	1160
86	S[10]	-1260	1160
87	S[9]	-1380	1160
88	S[8]	-1500	1160
89	S[7]	-1620	1160
90	S[6]	-1740	1160
91	S[5]	-1860	1160
92	S[4]	-1980	1160
93	S[3]	-2110	1160
94	S[2]	-2240	1160
95	S[1]	-2240	1030
96	V0	-2240	890
97	V2	-2240	750
98	V3	-2240	610
99	VSS	-2240	475
100	VDD	-2240	340
101	CL1	-2240	210
102	SHL1	-2240	80
103	SHL2	-2240	-50
104	CL2	-2240	-180
105	DL1	-2240	-310
106	DR1	-2240	-440
107	DL2	-2240	-580
108	DR2	-2240	-720
109	M	-2240	-860
110	S[49]	-2240	-1010

■ Functional Description :

Clock

The CL1 is the clock to latch data on the falling edge. It latches the data input from the bi-directional shift register at the falling edge of CL1 and transfers its outputs to the LCD driver circuit. The CL2 is the clock to shift data on the falling edge. It shifts the serial data at the falling of CL2 and transfers the output of each bit of the register to the latch circuit.

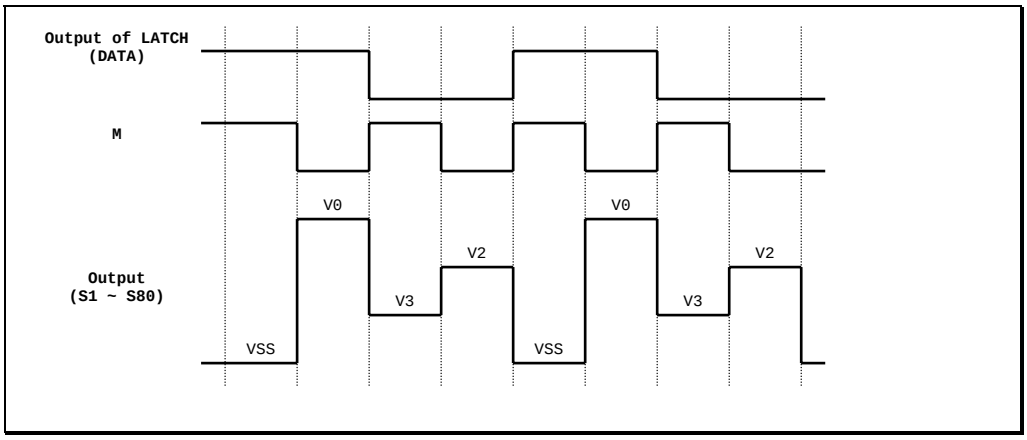
Shift Registers And Data I/O

The ST7921 supplies two sets of 48-bit shift register, which controls the shift direction by SHL1 & SHL2. The SHL1 controls the 1st 48-bit shift register, and SHL2 controls the 2nd 48-bit shift register. When SHL1 is connected to VDD, the 1st shift direction is from S48 to S1; when SHL1 is connected to VSS, the shift direction changes from S1 to S48. When SHL2 is connected to VDD, the 2nd shift direction is from S96 to S49; when SHL2 is connected to VSS, the shift direction changes from S49 to S96.
The DL1, DR1, DL2, DR2 are data input or output option function.

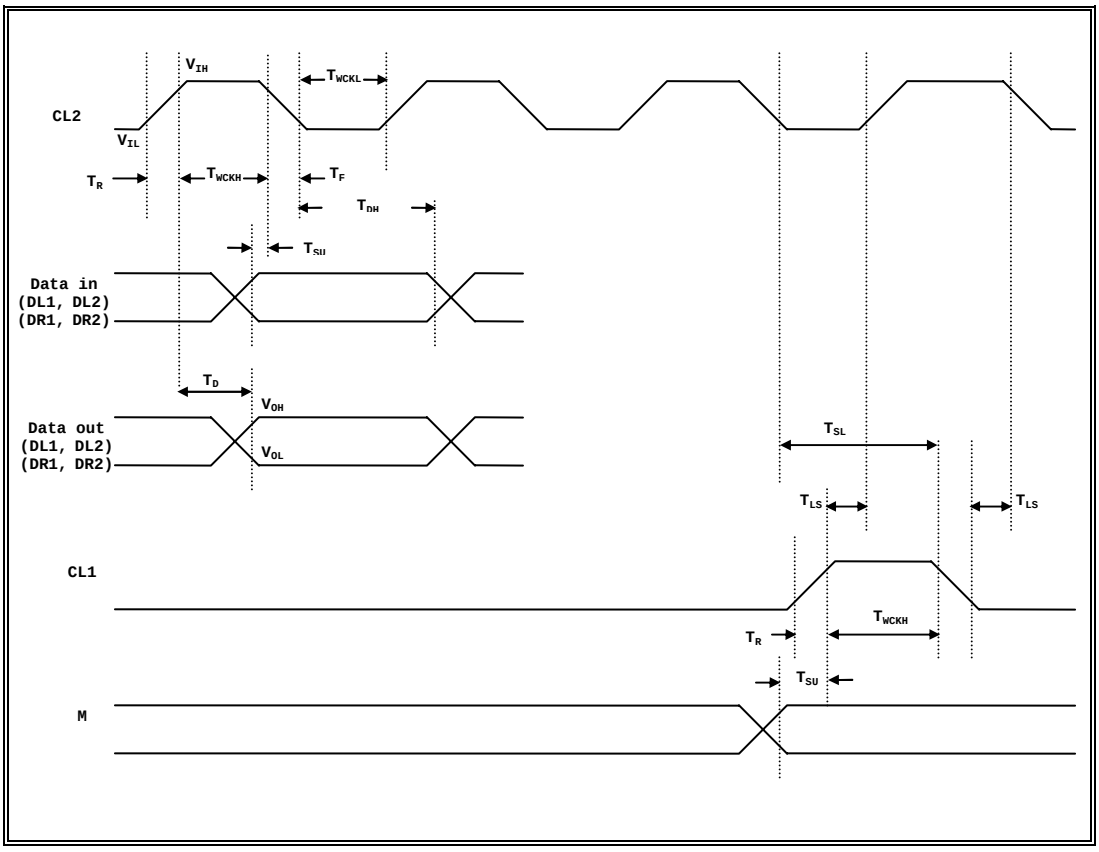
Shift Direction of Channel 1			
SHL1	Shift Direction	DL1	DR1
0	S1 → S48	IN	OUT
1	S48 → S1	OUT	IN

Shift Direction of Channel 2			
SHL2	Shift Direction	DL2	DR2
0	S49 → S96	IN	OUT
1	S96 → S49	OUT	IN

■ LCD Output Waveforms :



■ Timing Characteristics :



■ D.C Characteristics:

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit	Applicable pin
V_{DD}	Operating Voltage	-	2.7	-	5.5	V	-
V_{LCD}	Driver Supply Voltage	V_0-V_{SS}	3	-	7	V	-
V_{IH}	Input High Voltage	-	0.7V_{DD}	-	V_{DD}	V	CL1,CL2,M,SHL1,SHL2 DL1,DL2,DR1,DR2
V_{IL}	Input Low Voltage	-	0	-	0.3V_{DD}	V	
I_{LKG}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}	-5	-	5	uA	
V_{OH}	Output High Voltage	I_{OH} = -0.4mA	V_{DD}-0.4	-	-	V	DL1,DL2,DR1,DR2 V1~V4, S1~S80
V_{OL}	Output Low Voltage	I_{OL} = +0.4mA	-	-	0.4	V	
I_{DD}	Operating Current	F_{CL2} = 400K_{HZ}	-	280	460	uA	V_{DD},V_0
I_V	Leakage Current	V_{IN} = V_{DD} ~ V_{SS}	-10	-	10	uA	V1 ~ V4

■ A.C Characteristics :

Symbol	Parameter	Test Condition	Min.	Max.	Unit	Applicable pin
F_{CL}	Data Shift Frequency	-	-	400	K_{HZ}	CL2
T_{WCKH}	Clock High Level Width	-	800	-	ns	CL1,CL2
T_{WCKL}	Clock Low Level Width	-	800	-	ns	CL2
T_{SL}	Clock Set-up Time	CL2 → CL1	500	-	ns	CL1,CL2
T_{LS}	Clock Set-up Time	CL1 → CL2	500	-	ns	CL1,CL2
T_R/T_F	Clock Rise/Fall Time	-	-	200	ns	CL1,CL2
T_{SU}	Data Set-up Time	-	300	-	ns	DL1,DL2,DR1,DR2
T_{DH}	Data Hold Time	-	300	-	ns	DL1,DL2,DR1,DR2
T_D	Data Delay Time	CL = 15 $_P$F	-	500	ns	DL1,DL2,DR1,DR2

■ Maximum Absolute Ratings :

Symbol	Parameters	Min.	Max.	Unit
V_{DD}	Supply Voltage	-0.3	7	V
T_{OPR}	Operating Temperature	-20	75	^{0}C
T_{STG}	Storage Temperature	-55	125	^{0}C

■ Application Circuit : (2Line x 16 Chinese Word)